WHAT IS CLAIMED IS:

1. A semiconductor chip package comprising:

at least a semiconductor chip;

at least a chip carrier having a front surface to which said chip is attached, and having a back surface, at least a via, and a plurality of edges;

at least a bonding finger formed on the front surface of said chip carrier to electrically connect said chip;

at least a metal pad attached to the back surface of said chip carrier;

at least a first conduction line formed on the front surface of said chip carrier to connect said bonding finger and said metal pad through said via; and

at least a second conduction line formed on the front surface of said chip carrier, with a first end thereof on an edge of said chip carrier, and a second end thereof connecting said first conduction line to be electrically connecting to said bonding finger, said second conduction line for conducting to said bonding finger the electrical current applied to the first end thereof for plating material on said bonding finger.

2. The semiconductor chip package according to claim 1 wherein said first conduction line is for conducting signals between said bonding finger and said metal pad.

3. The semiconductor chip package according to claim 2 wherein said first conduction line includes a conducting-auxiliary-path which is the part of said first conduction line between said bonding finger and the second end of said second conduction line, said conducting-auxiliary-path for conducting, when plating material on said bonding finger, said electrical current from the second end of said second conduction line to said bonding finger.

4. The semiconductor chip package according to claim 1 wherein said first conduction line is left from dividing a large sheet of interim product into a plurality of said chip carriers.

5. The semiconductor chip package according to claim 1 further comprising a chip-electrical-connector for said bonding finger to electrically connect said chip.

6. The semiconductor chip package according to claim 5 wherein said chip-electrical-connector is an electrical wire.

7. The semiconductor chip package according to claim 5 wherein said chip is a flip chip and said chip-electrical-connector is a bump of said chip.

8. The semiconductor chip package according to claim 5 further comprising at least an encapsulation layer covering said chip, said bonding finger, said first conduction line, said second conduction line, and said chip-electrical-connector.

9. The semiconductor chip package according to claim 3 wherein said conducting-auxiliary-path and said second conduction line are such that the total length of said conducting-auxiliary-path and said second conduction line is longer than the distance between said bonding finger and an edge of said chip carrier which is closest to said bonding finger.

10. A semiconductor chip package comprising:

at least a semiconductor chip;

at least a chip carrier having a front surface to which said chip is attached, and a plurality of edges;

at least a bonding finger formed on the front surface of said chip carrier to electrically connect said chip, and having a first line and a second line, the first line thereof facing a selected edge of said chip carrier, and the second line being perpendicular to the selected edge of said chip carrier;

and

at least a plating-conduction-line formed on the front surface of said chip carrier to have one end thereof on the selected edge of said chip carrier and another end thereof connecting said bonding finger via the second line of said bonding finger.

11. The semiconductor chip package according to claim 10 further comprising a chip-electrical-connector for said bonding finger to electrically connect said chip.

12. The semiconductor chip package according to claim 11 wherein said chip-electrical-connector is an electrical wire.

13. The semiconductor chip package according to claim 11 wherein said chip is a flip chip and said chip-electrical-connector is a bump of said chip.

14. The semiconductor chip package according to claim 10 wherein said chip carrier further comprises at least a via and a back surface.

15. The semiconductor chip package according to claim 14 further comprising at least a metal pad attached to the back surface of said chip carrier, and at least a trace connecting said bonding finger and said metal pad through said via.

16. The semiconductor chip package according to claim 11 further comprising at least an encapsulation layer covering said chip, said chip-electrical-connector, said bonding finger, and said plating-conduction-line.

17.A semiconductor chip package comprising:

at least a semiconductor chip;

at least a chip carrier having a front surface to which said chip is attached, and having a back surface, at least a via, and a plurality of edges;

at least a bonding finger formed on the front surface of said chip carrier to electrically connect said chip;

at least a metal pad attached to the back surface of said chip carrier;

at least a first conduction line formed on the front surface of said chip carrier to connect said bonding finger and said metal pad through said via; and

at least a second conduction line formed on the front surface of said chip carrier, with a first end thereof on an edge of said chip carrier, and a second end thereof connecting said first conduction line to be electrically connecting to said bonding finger, said second conduction line being left on said chip carrier after conducting to said bonding finger the electrical current applied to the first end thereof for plating material on said bonding finger.